IN THE CLAIMS

1. (Currently Amended) A dual-data rate (DDR) synchronous dynamic random access memory (SDRAM)/synchronous graphic random access memory (SGRAM) comprising a single memory device comprising:

a memory array including a quad-bank DRAM; and,

a logic circuitry coupled to the memory array configurable to operate the single memory device in a first operational mode having delayed lock loop (DLL) capability and in a second operational mode having non-DLL capability.

2. (Original) The DDR SDRAM/SGRAM of claim 1, wherein the DLL capability provides for alignment of an output data on a read line of the DDR SDRAM/SGRAM with an incoming clock signal.

3. (Currently Amended) ~~The DDR SDRAM/SGRAM of claim 1,~~ A dual-data rate (DDR) synchronous dynamic random access memory (SDRAM)/synchronous graphic random access memory (SGRAM) comprising a single memory device comprising:

a memory array including a quad-bank DRAM; and,

a logic circuitry coupled to the memory array configurable to operate the single memory device in a first mode having delayed lock loop (DLL) capability and in a second mode having non-DLL capability;

wherein the logic circuitry comprises an Extended Mode Register, defaults to the second mode having the non-DLL capability, and enters the first mode having the DLL capability upon receiving a Load Mode Register command on the Extended Mode Register.

4. (Original) The DDR SDRAM/SGRAM of claim 1, wherein the single memory device has a plurality of characteristics that vary according to operation in the first mode having the DLL capability compared to operation in the second mode having the non-DLL capability, the

plurality of characteristics including at least one characteristic selected from the group essentially consisting of: DLL, CAS latencies, preambles, postambles, set-up timing and hold timing.

5. (Currently Amended) A memory device for graphics processing comprising:

a memory array including an internal pipelined DRAM;

a logic circuitry coupled to the memory array configurable to operation in a first operational mode having delayed lock loop (DLL) capability and in a second operational mode having non-DLL capability,

wherein the DLL capability provides for alignment of an output data on a read line of the memory array with an incoming clock signal.

6. (Currently Amended) ~~The memory device of claim 5,~~ A memory device for graphics processing comprising:

a memory array including an internal pipelined DRAM;

a logic circuitry coupled to the memory array configurable to operation in a first mode having delayed lock loop (DLL) capability and in a second mode having non-DLL capability,

wherein the DLL capability provides for alignment of an output data on a read line of the memory array with an incoming clock signal; and

wherein the logic circuitry comprises an Extended Mode Register, defaults to the second mode having the non-DLL capability, and enters the first mode having the DLL capability upon receiving a Load Mode Register command on the Extended Mode Register.

7. (Original) The memory device of claim 5, wherein the memory device has a plurality of characteristics that vary according to operation in the first mode having the DLL capability compared to operation in the second mode having the non-DLL capability, the plurality of characteristics including at least one characteristic selected from the group essentially consisting of: DLL, CAS latencies, preambles, postambles, set-up timing and hold timing.

8. (Currently Amended) A system comprising:

a processor; and,

a dual-data rate (DDR) memory having a single memory device including a quad-bank DRAM and configurable to operate in a first operational mode and a second operational mode, the first operational mode and the second operational mode each relating to a different alignment of output data as to a read line of the memory for different industry standard operational modes for memory devices.

9. (Original) The system of claim 8, wherein the first mode includes a delayed lock loop (DLL) capability and the second mode includes a non-DLL capability.

10. (Original) The system of claim 8, wherein the first mode includes a phase lock loop (PLL) capability and the second mode includes a non-PLL capability.

11. (Currently Amended) A dual-data rate (DDR) memory comprising a single memory device comprising:

a memory array including a quad-bank DRAM; and,

a logic circuitry coupled to the memory array configurable to operate in a first operational mode and a second operational mode, the first mode and the second mode each relating to a different alignment of output data as to a read line of the memory for different industry standard operational modes for memory devices.

12. (Original) The DDR memory of claim 11, wherein the first mode relates to one of a delayed lock loop (DLL) capability and a phase lock loop (PLL) capability.

13. (Currently Amended) A dual-data rate (DDR) memory device comprising:

a memory array including full page burst capability;

a logic circuit coupled to the memory array configurable to operate in a first operational mode and a second operational mode, the first mode and the second mode each relating to a

different alignment of output data as to a read line of the memory device for different industry standard operational modes for memory devices.

14. (Original) The DDR memory device of claim 13, wherein the memory device comprises a synchronous dynamic random access memory (SDRAM)/synchronous graphic random access memory.

15. (Currently Amended) A memory device comprising:

a memory array including a quad-bank DRAM having full page burst capability;

a logic circuit coupled to the memory array and having a capability to align output data as to a read line of the memory device in accordance with a plurality of different industry standard memory device operational modes.

16. (Currently Amended) The memory device of claim 15, wherein the plurality of different industry standard memory device operational modes includes a delayed lock loop (DLL) mode.

17. (Currently Amended) The memory device of claim 15, wherein the plurality of different industry standard memory device operational modes includes a phase lock loop (PLL) mode.

18. (Currently Amended) The memory device of claim 15, wherein the plurality of different industry standard memory device operational modes includes two modes.

19. (Original) The memory device of claim 15, wherein the memory device comprises a synchronous dynamic random access memory (SDRAM)/synchronous graphic random access memory.

20. (Currently Amended) A system comprising:

a processor; and,

a dual-data rate (DDR) memory having a single memory device having full page burst capability and a capability to align output data as to a read line of the memory device in accordance with a plurality of different industry standard memory device operational modes.

21. (Original) The system of claim 20, wherein the plurality of different industry standard memory device operational modes includes a delayed lock loop (DLL) mode.

22. (Original) The system of claim 20, wherein the plurality of different industry standard memory device operational modes includes a phase lock loop (PLL) mode.

23. (Original) The system of claim 20, wherein the plurality of different industry standard memory device operational modes includes two modes.

24. (Original) The system of claim 20, wherein the memory device comprises a synchronous dynamic random access memory (SDRAM)/synchronous graphic random access memory.

25. (New) The DDR SDRAM/SGRAM of claim 3, wherein the single memory device has a plurality of characteristics that vary according to operation in the first mode having the DLL capability compared to operation in the second mode having the non-DLL capability, the plurality of characteristics including at least one characteristic selected from the group essentially consisting of: DLL, CAS latencies, preambles, postambles, set-up timing and hold timing.

26. (New) The DDR SDRAM/SGRAM of claim 3, wherein the DLL capability provides for alignment of an output data on a read line of the DDR SDRAM/SGRAM with an incoming clock signal.

27. (New) The memory device of claim 6, wherein the memory device has a plurality of characteristics that vary according to operation in the first mode having the DLL capability compared to operation in the second mode having the non-DLL capability, the plurality of characteristics including at least one characteristic selected from the group essentially consisting of: DLL, CAS latencies, preambles, postambles, set-up timing and hold timing.